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*Iwasaki, K.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 7 , Issue: 1 , Jan. 1988

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### 2 A flexible logic BIST scheme and its application to SoC designs

*Xiaoqing Wen; Hsin-Po Wang;*

Test Symposium, 2001. Proceedings. 10th Asian , 19-21 Nov. 2001

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### 3 A cost-effective scheme for at-speed self-test

*Xiaowei Li; Fuqing Yang;*

TENCON '93. Proceedings. Computer, Communication, Control and Power Engineering.1993 IEEE Region 10 Conference on , Issue: 0 , 19-21 Oct. 1993

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### 4 Self-testing and self-reconfiguration architecture for 2-D WSI arrays

*Abujbara, H.Y.; Al-Arian, S.A.;*

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### 5 E-BIST: enhanced test-per-clock BIST architecture

*Son, Y.; Chong, J.; Russell, G.;*

Computers and Digital Techniques, IEE Proceedings- , Volume: 149 , Issue:

1, Jan. 2002

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Communications, Computers and signal Processing, 2001. PACRIM. 2001 IEEE Pacific Rim Conference on, Volume: 1, 26-28 Aug. 2001

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[\[Abstract\]](#) [\[PDF Full-Text \(780 KB\)\]](#) IEEE CNF**10 Module level weighted random patterns***Savir, J.;*

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Circuits and Systems, 1990., IEEE International Symposium on, 1-3 May 1990

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Circuits and Systems, 1990., IEEE International Symposium on, 1-3 May 1990

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